

CLAIMS

1. (Currently amended) A process to improve adhesion of dielectric materials to a metal layer, comprising:

providing an unpatterned metal layer having a first major surface, wherein the metal layer comprises a layer of copper and a layer of a second metal or alloy;

micro-roughening the first major surface to form a micro-roughened surface; and etching the metal layer to form a circuit pattern in the metal layer, wherein the micro-roughening is carried out prior to the etching,

wherein the micro-roughening is carried out by applying a mixture comprising water, acid, an oxidant and a corrosion inhibitor to the unpatterned metal layer,

and wherein from about 0.5 to about 2 microns of metal is removed from the first major surface in the micro-roughening step.

2. (Original) The process of claim 1, wherein the unpatterned metal layer is not treated to increase surface roughness prior to the micro-roughening.

3. (Original) The process of claim 1, wherein the micro-roughened surface is not subjected to a further roughening following the etching.

4. (Original) The process of claim 1, wherein the circuit pattern formed by the etching has a cross-sectional area, and the cross-sectional area is not substantially further reduced subsequent to the etching.

5. (Original) The process of claim 1, further comprising cleaning the first major surface prior to the micro-roughening.

6. (Original) The process of claim 5, further comprising pre-conditioning the first major surface comprising applying a solution comprising a water soluble alcohol subsequent to the cleaning and prior to the micro-roughening.

6. (Original) The process of claim 6, wherein the solution further comprises a corrosion inhibitor.

8. (Original) The process of claim 1, further comprising steps of applying an etch resist to the micro-roughened surface and patterning the etch resist prior to the etching.

9. (Original) The process of claim 1, further comprising removing the etch resist subsequent to the etching.

10. (Original) The process of claim 1, further comprising applying a secondary metal coating to the circuit pattern.

11. (Original) The process of claim 1, further comprising applying a dielectric material to the circuit pattern.

12. (Previously presented) The process of claim 1, wherein the metal layer displays a galvanic edge effect only at outermost edges of the metal layer prior to the etching.

13. (Previously presented) The process of claim 1 wherein subsequent to the etching, elements of the circuit pattern are substantially free of a galvanic edge effect.

14. (Previously presented) The process of claim 1, wherein the second metal is an alloy of iron and nickel.

15. (Previously presented) The process of claim 14, wherein the alloy comprises about 64 atomic percent iron and about 36 atomic percent nickel.

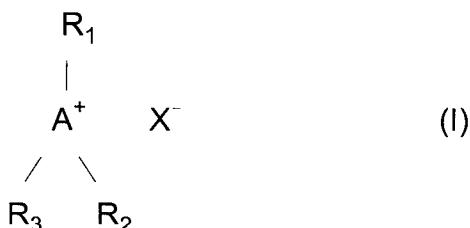
16. (Previously presented) The process of claim 1, wherein the oxidant comprises hydrogen peroxide and the corrosion inhibitor comprises benzotriazole and the acid comprises sulfuric acid.

17. (Previously presented) The process of claim 1, wherein the acid comprises one or more of sulfuric acid, hydrochloric acid, a sulfonic acid, or an organic acid.

18. (Previously presented) The process of claim 1, wherein the oxidant comprises one or more of a peroxide, a peracid, a halide, a nitrate, cupric ion or ferric ion.

19. (Withdrawn) The process of claim 1, wherein the corrosion inhibitor comprises at least one nitrogen-containing, five-membered heterocyclic compound which does not contain any sulphur, selenium or tellurium atom in the heterocycle.

20. (Withdrawn) The process of claim 1, wherein the mixture further comprises at least one adhesive compound from the group consisting of sulfinic acids, seleninic acids, tellurinic acids, heterocyclic compounds containing at least one sulphur, selenium and/or tellurium atom in the heterocycle, and sulfonium, selenonium and telluronium salts having the general formula (I),



wherein in formula (I) A is S, Se or Te; R₁, R₂ and R₃ are independently C₁-C₆ alkyl, substituted alkyl, alkenyl, phenyl, substituted phenyl, benzyl, cycloalkyl, substituted cycloalkyl, R₁, R₂ and R₃ being the same or different; and X⁻ is an anion of an inorganic or organic acid or hydroxide, provided that the acid selected to constitute component (b) is not identical to the sulfinic, seleninic or tellurinic acids selected as component (d).

21. (Cancelled)

22. (Previously presented) The process of claim 1, wherein the oxidant comprises 0.1 to 20% by weight hydrogen peroxide and wherein the mixture further comprises a surfactant.

23-24. (Cancelled)

25. (Original) The process of claim 1, wherein the micro-roughened surface has a surface roughness r_a as measured by profilometer from about 0.1 to about 0.5 microns.

26. (Original) The process of claim 1, wherein the micro-roughened surface covers about 90% or more of the first major surface.

27. (Original) The process of claim 1, wherein the micro-roughened surface covers substantially all of the first major surface.

28. (Currently amended) A process to improve adhesion of dielectric materials to a metal layer, comprising:

- a. providing an unpatterned metal layer having a first major surface, wherein the metal layer comprises a layer of copper and a layer of a second metal or alloy;
- b. micro-roughening the unpatterned metal layer with a micro-roughening solution to form a micro-roughened surface on the first major surface;
- c. applying an etch resist to the micro-roughened surface;
- d. patterning the etch resist to reveal areas of metal to be removed;
- e. etching the metal layer which is not protected by the etch resist to form a circuit pattern; and
- f. removing the etch resist,

wherein the micro-roughened surface is not subjected to a further roughening following (f),
wherein from about 0.5 to about 2 microns of metal is removed from the first major surface in the micro-roughening step.

29. (Original) The process of claim 28, wherein the unpatterned metal layer is not treated to increase surface roughness prior to the micro-roughening.

30. (Original) The process of claim 28, wherein the circuit pattern formed by the etching has a cross-sectional area, and the cross-sectional area is not substantially further reduced subsequent to the etching.

31. (Original) The process of claim 28, further comprising applying a secondary metal coating to the circuit pattern.

32. (Original) The process of claim 28, further comprising applying a dielectric material to the circuit pattern.

33. (Previously presented) The process of claim 28, wherein the metal layer displays a galvanic edge effect only at outermost edges of the metal layer prior to the etching.

34. (Previously presented) The process of claim 28, wherein subsequent to the etching, elements of the circuit pattern are substantially free of a galvanic edge effect.

35. (Original) The process of claim 28, wherein the metal layer is CIC.

36. (Currently amended) A process to improve adhesion of dielectric materials to a metal layer, comprising:

a. providing an unpatterned metal layer having a first major surface, wherein the metal layer comprises a layer of copper and a layer of a second metal or alloy;

b. micro-roughening the unpatterned metal layer with a micro-roughening solution to form a micro-roughened surface on the first major surface;

c. applying an etch resist to the micro-roughened surface;

d. patterning the etch resist to reveal areas of metal to be removed;

e. etching the metal layer which is not protected by the etch resist to form a circuit pattern;

f. removing the etch resist;

g. optionally applying a secondary metal coating to the micro-roughened surface; and

h. applying a dielectric to the micro-roughened surface.

wherein from about 0.5 to about 2 microns of metal is removed from the first major surface in the micro-roughening step.

37. (Original) The process of claim 36, wherein the unpatterned metal layer is not treated to increase surface roughness prior to the micro-roughening.

38. (Original) The process of claim 36, wherein the micro-roughened surface is not subjected to a further roughening following (f).

39. (Original) The process of claim 36, wherein the circuit pattern formed by the etching has a cross-sectional area, and the cross-sectional area is not substantially further reduced subsequent to the etching.

40. (Original) The process of claim 36, further comprising applying a secondary metal coating to the circuit pattern.

41. (Previously presented) The process of claim 36, wherein the metal layer displays a galvanic edge effect only at outermost edges of the metal layer prior to the etching.

42. (Previously presented) The process of claim 36, wherein subsequent to the etching, elements of the circuit pattern are substantially free of a galvanic edge effect.

43. (Original) The process of claim 36, wherein the metal layer is CIC.